## REMARKS

### Allowable Subject Matter

The Applicant gratefully acknowledges the indication of allowable subject matter in claims 5-10. Each of claims 5 and 6 is now rewritten in independent form to include the limitations of claims 1 and 2. Claims 7-10 depend directly or indirectly from claim 6. All of claims 5-10 as now presented are believed to be in condition for allowance.

### Rejection Under 35 USC §103(a)

Claims 1-4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Toeppen *et al.* U.S. Patent No. 5,900,755 ("Toeppen"):

> "Regarding Claim 1, Toeppen discloses (Figures 1 and 5) a method of calibrating a timer acquisition clock generator 114 by adjusting through an offset, having coarse measurement scaled acquisition clock 518 in which time intervals are defined by the time period of clock 518 as boundaries and a fine measurement reference clock signal 502, in which time between boundaries is interpolated using a voltage ramp analog input 116, the method comprising:
>
> "Determining alignment of a voltage ramp analog input 116 (Figure 1 and 2) relative to the reference clock signal 502 having a known relationship to the time boundaries, also shown in (Figure 5).
>
> "Sampling the voltage ramp analog input 116 (Figures 1 and 2), with acquisition clock 124 (Figure I), which is the same as the acquisition clock 514 (Figure 5) at a plurality of known times, in relationship to the time boundaries of scaled acquisition clock 51 8 and reference clock signal 502.
>
> "Toeppen does not determine the slope of the voltage ramp from the voltage samples. However, he stores in a memory 106 the digital waveform samples 120 and then he displays waveform (Figure 3), which is a plot of many welldistributed samples of the input waveform (Figure 2). The displayed waveform is a saw-toothed type with two ramps having a positive and negative slope, respectively. The slope is a function of sample distribution. It would have been obvious at the

time the invention was made to a person having ordinary skill in the art to use the digital waveform samples, in the device of Toeppen, in order to calculate the slope of a ramp waveform, since storing digital samples allows a visual display of the waveform.

"Regarding Claim 2, aligning the voltage ramp analog input 116 (Figure 1 and 2) relative to the time interval boundaries of the reference clock signal 502, also (Figure 5)

"Regarding Claims 3, 4, Toeppen defines the time intervals by clock 518 at a first frequency defined by a frequency divider 512 (Figure 5), further comprising a phase locked loop phase detector 504, which compares clock 518 to the reference clock 502 at second frequency, where the output of the phase detector 520 defines the phase relationship between the reference clock 502 and the acquisition clock 51 8, described in (column 3, lines 5-20). "

Reconsideration of the rejection of claims 1-4 is respectfully requested.

Toeppen is concerned with the acquisition of digital waveform data, e.g., of time-varying waveforms for display on a digital oscilloscope.

Toeppen recognizes that a sampling clock of fixed phase and frequency may be accidentally in a simple relationship to the signal to be sampled. An unwanted consequence is that the same parts of the signal are sampled many times, while some parts are not sampled at all. (See Toeppen Figure 4 and column 2, line 62 - column 3, line 5.)

Toeppen proposes to break this accidental synchronization by applying random phase offsets to the phase locked loop used to generate the sampling clock:

"The preferred embodiment is a method and apparatus for preventing correlation between a waveform being sampled and the acquisition clock of a digital oscilloscope by modulating the phase of the acquisition clock. The acquisition clock is generated by a phase locked loop. The phase of the acquisition clock is modulated by adding an offset to the input of the phase locked loop's loop filter.

> The offset is generated by inputting values to the input of a digital-to-analog converter. The output of the digital-to-analog converter is changed between acquisition cycles. The values are input to the DAC are generated by software executing on a microprocessor. In another preferred embodiment, the acquisition clock is generated by a delay locked loop and the phase of the acquisition clock is modulated by adding an offset to the input of the delay locked loop's loop filter." (Toeppen column 2, lines 10-26.)

Toeppen's Figure 1 shows a digital sampling system (as used for a digital storage oscilloscope) which takes samples of an analog input at a rate set by acquisition clock generator 114. Toeppen's Figures 5 and 6 show acquisition clock generator 114 in more detail.

Referring to Toeppen's Figure 1, generally the acquisition clock generator 114 is running asynchronously to the repetition rate of the analog signal to be sampled. A stored "image" of the analog signal is built up over many repetitions of the signal by clock 114 taking samples essentially at random. The exact time positions of each of these samples is measured by time interpolator 112. The CPU 108 can then assemble the samples in the correct time positions for display. (Toeppen column 2, lines 27-44.)

Contrary to the assertion in the Office Action, Toeppen is not concerned with "calibrating a timer acquisition clock." Nothing in the Toeppen patent is concerned with calibrating anything.

Also, Toeppen's signal 116 is not identified as a voltage ramp input – instead, it is the analog input of a digital sampling system (e.g., a digital oscilloscope) and can be ANY signal. For example, Toeppen describes Figure 2 as an example input signal which in the example given is a sawtooth (triangle) wave.

It is repectfully submitted that Toeppen fails to teach or suggest the invention defined in Applicant's claims 1-4.

As to claim 1, Toeppen fails to teach or suggest anything at all with respect to "calibrating a timer having a coarse measurement capability in which time intervals defined by boundaries are counted and a fine measurement capability in which time between boundaries is interpolated using a voltage ramp."

Further regarding claim 1, Toeppen fails to teach or suggest "determining alignment of the voltage ramp" of a timer " relative to a reference-clock signal having a known relationship to the boundaries" defining timing intervals of a timer.

Still further regarding claim 1, Toeppen fails to teach or suggest "sampling the voltage ramp" of a timer "at a plurality of known times relative to the boundaries."

Still further regarding claim 1, Toeppen fails to teach or suggest "determining slope of the voltage ramp" of a timer "as a function of time from the voltage samples."

As to claim 2, Toeppen fails to teach or suggest "aligning the voltage ramp" of a timer " relative to the time interval boundaries."

As to claim 3, Toeppen fails to teach or suggest the method of claim 2 in which "the time intervals are defined by an interval clock signal at a first frequency, further comprising phase-locking the interval clock signal to a reference-clock signal at a second frequency so that phase relationship between the interval-clock signal and the reference-clock signal is defined."

As to claim 4, Toeppen fails to teach or suggest the method of claim 3 "wherein phase-locking comprises operating a phase-locked loop to maintain a defined phase relationship between the interval-clock signal and the reference-clock signal."

It is respectfully submitted that a fair reading of Toeppen without the benefit of hindsight knowledge of Applicant's invention would not suggest to one of skill in the art the invention defined in Applicant's claims 1-4 at the time the invention was made. As noted at MPEP §2141.01:

> "It is difficult but necessary that the decisionmaker forget what he or she has been taught . . . about the claimed invention and cast the mind back to the time the invention was made (often as here many years), to occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art." *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

Formal Drawings

Formal drawings were submitted with a Transmittal on May 25, 2002. A return receipt card has been received.

However, the formal drawings have not been acknowledged in the Official Action of July 15, 2003 and were not included in the publication of the present application (Patent Application Publication US 2003/0141879 A1 dated July 31, 2003.)

Acknowledgment of the formal drawings is respectfully requested.

Fees

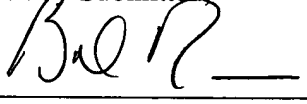
The Commissioner is hereby authorized to charge fees under 37 CFR §1.17 that may be required, or credit any overpayment, to deposit Account No. 19-0603 maintained in the name of NPTest, LLC. A duplicate of this paper is enclosed.

Conclusion

The application is now believed to be in condition for allowance and such action is respectfully urged. The Examiner is respectfully requested to contact the undersigned by telephone should there be any further issue preventing allowance.

January 13, 2004

Respectfully Submitted,



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